Action Item No.	Subsystem	Issue	Recommendation	Response	Reviewer	Responsibility	Due Date
1	GARC	Current Density for Power Distribution in metal busses.	Review Design Rules for fab to determine if the metal widths, and contact density between metal layers meet process specs at operating temperatures. Rule of thumb: ~1mA/µm of wire @ room temp. Feel free to contact with similar numbers for typical fab.	Haller - is part of check before submission. Conforms to Agilent spec. For details see item (4) in attached word file (Martin-Haller doc, see tab below)). Sheppard (8/15/02) - We should still make a note to re-check this parameter prior to submission of GARC V2.	Mark N. Martin	D. Sheppard (answered by G. Haller)	08/16/02
2	GARC	Latch-up issue on LVDS I/O cells. Cells have not been tested for latch-up. High current density make these cells more likely to see latch-up	LVDS cells should be tested for latch-up	Radiation test for similar chip meets radiation requirements. However 3.5mA driver is above 1mA on other chips. All ASICs need to be rad tested, is parts control requirement. For details see (5). Unger (8/15/02) - planning radiation testing on GAFE (2nd gen) and GARC (1st gen) after 10/02	Mark N. Martin	G. Haller, N. Virmani, G. Unger	08/16/02
3	GARC	Latch-up testing? Analog and digital chips. Especially is the LVDS drivers. Latch-up protection? Housekeeping of the boards for latch-up?	Have the LVDS drivers tested for latch-up. Fix the LVDS design if it latches for the HP0.5µ process. Possibly allow current monitor for latch-up detectors	see response in action item 3 above	Nick Paschalidis	G. Haller, N. Virmani, G. Unger	08/16/02
4	GARC	Power bus current capability concerns. Meta1 current density, is it enough to carry the LVDS 300mA? Typical current density of M1 is 1-2mA/µ width.	Check with HP about the current density profile of M layers as a function of temperature. Make sure that in every path the current does not exceed the current limit. ?? properly the metal widths.	Haller - is part of check before submission. See item (4) in write-up (Martin-Haller doc, see tab below)) (by the way not all drivers are routed together). Sheppard (8/15/02) - This is the same issue as item #1.	Nick Paschalidis	G. Haller, D. Sheppard (answered by G. Haller)	08/16/02
5	GARC	Stuck-at fault analysis and testing IDDQ	Testing: Functional testing, Stack at fault testing, IDDQ testing	Bob and I have discussed this testing. We agree that it is a good idea and will build GSE or modify GSE to accommodate these tests. I will also generate a written plan for GARC testing.	Nick Paschalidis	D. Sheppard	08/16/02

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6	GAFE	Resistive N-well is not a good approach. Temp, power supply and signal could affect resistance ber square. How many ADC bits are required? Sample and Hold charge injection. Radiation dose to charge the N-well resistor values.	Use poly-silicide resistors instead of N-well.	Singh: N well resistances were used as the values required are quiet large, like 220K, etc. The resistive values are large because the time constants are large, 3 us for the shaping time. Temp Stability: The prototype ASIC was temperature cycled from +50 C down to -20 C and the gain variation in the high gain channel was about 6% and in the Low gain channel was about 6.5% over the entire temp range. The resolution requirements for the Low Engergy (High Gain Channel) is 0.02 Mip or 5% which ever is larger, this implies a resolution of 4 to 5 bits. The resolution requirements for the High Engergy (Low Gain Channel) is 1 Mip or 2% which ever is larger, this implies a resolution of 5 to 6 bits. The N well resistances seem adequate for the requirements, therefore they were used since they take 4 to 6 times less area than the silicide blocked poly resistors. Singh (8/15/02) - will be looking into changing the resistors in the shaping amps with Silicide Blocked Poly resistors.	Nick Paschalidis	S. Singh	08/16/02

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7	GAFE	Resistor charge splitting. High resistor values are not good.	Consider using smaller value resistors.	Singh:I agree with this suggestion as also indicated by the slide presented by me in the review that showed good linearity with low value input resistance, the degradation in linearity at higher resistances is probably due to the increased effect of parasitic capacitances and larger pickup. I will be looking into this further to see how much the resistance values can be lowered.	Nick Paschalidis	S. Singh	08/16/02
8	GAFE	System level noise. What is actual system level noise performance? What is the requirement?	Investigate power supply noise performance and power supply rejection of amplifiers to determine if performance is satisfactory.	Singh: The noise requirement is that it be less than 0.1 MIP. As shown in one of my slides, the noise measured on the prototype ASIC is 0.01 MIP. Once the engineering system is built, noise further down the electronics chain, that is after the ADC will also be measured.	Mike Johnson	S. Singh, G. Unger	08/16/02
9	GAFE	PHA accuracy. Circuit response will vary with temperature, power supply bias and signal level.	Verify error budget due to circuit/system variability is not exceeded.	The thermal cycling of Track and Hold output was temperature cycled over -20 to + 50 C and the gain of the PHA channel was found to change by less than 10 %	Mike Johnson	G. Unger	08/16/02
10	GARC	State machine design. Default Exemplar state machines are not desirable for flight designs. SEU effects can send machine to invalid states.	Implement state machines with gray coding. Either ensure invalid state logic is not removed during optimization, or disable state machine optimization.	If we do reroute the GARC or GAFE cores, we will set the Exemplar synthesis to One Hot encoding (DAS). Was considered (as always) but is not needed. See item 5, write up for details. (FYI to the ACD FREE we use time-outs and not hand-shake, time-outs are handled in hardware/software for such and many other occasions) Sheppard (8/15/02) - GARC can use the One Hot encoding. We do use hand-shaking in the GARC logic.	Mike Johnson	D. Sheppard	08/16/02

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11	GARC	System level design. GARC design is per SLAC requirements, but SLAC requirements do not seem to address flight system issues. e.g. latchup susceptibility, housekeeping/status.	Pass system concerns that would affect subsystem operation up to SLAC. GSFC has in-house expertise that should be leveraged.	1) it is addressed, see item (6) and (7) in write-up	Mike Johnson	G. Shiblie	08/16/02
12	GARC	Single-bit flips due to radiation or supply voltage fluctuations can cause the state machines to enter undefined states or defined states that are not the one's expected (e.g. jump to a state waiting for a handshake signal that won't arrive).	Consider switching state machines to one – hot or TMR encoding. Make sure the synthesis tool does not optimize out the 'default' case. Set a status bit in the default state which informs the instrument that a state machine error has occurred and/or have that status bit reset the chip into a safer mode.	Agreed. We will add status bits to the state machines and ensure the default cases are not optimized out (DAS). Was considered (as always) but is not needed. See item 5, write-up for details. (FYI to the ACD FREE we use time-outs and not hand-shake, time-outs are handled in hardware/software for such and many other occasions). Sheppard (8/15/02) - I'm not sure where the second part of this comment comes from. It doesn't seem to apply to this item. This is a good suggestion; originally I had not considered them, so that is inaccurate.	Ken Wagner	D. Sheppard	08/16/02